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Design of a Low Power Combinational Circuit by using Adiabatic Logic

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Abstract-
A novel low power and Positive Feedback Adiabatic Logic (PFAL) combinational low power circuit is presented in this paper. The power consumption and general characteristics of the PFAL combinationallow power circuit arethen compared against two combinational low power circuit Efficient Charge Recovery Logic (ECRL), Conventional CMOS. The proposed PFAL combinational low power circuit design was proven to be superior to the other two designs in power dissipation and area. The combination of low power and low transistor count makes the new PFAL cell a viable option for low power design.
Keywords -Adiabatic Logic, Power Dissipation, power clock.

I.INTRODUCTION

Adiabatic logic is an attractive low-power approach by utilizing AC voltage supplies (power-clocks) to recycle the energy of circuits instead of being dissipated as heat. Several adiabatic logic architectures, such as ECRL (Efficient Charge Recovery Logic, it consists of one cross coupled PMOS transistors for precharge and evaluate), PFAL (Positive Feedback Adiabatic Logic), have been reported and achieved considerable energy savings. Static CMOS circuits don't exist any direct path between the power supply and ground rails under steady-state operating conditions. The absence of current flow (ignoring leakage currents) means that the circuits don't consume any static power. However, in the adiabatic circuits, energy dissipation occurs even for constant input signals, because their output nodes are always charged and discharged by power-clocks, so that the energy savings of the adiabatic circuits are limited. In conventional CMOS circuits, disabling the power supply for the inactive portions of the circuits is a useful approach for power dissipation reduction. Similarly, idle adiabatic logic blocks can be also shut down by switching off its power-clocks. Several power-gating schemes for adiabatic circuits have been proposed. Used the bootstrapped complementary NMOS switches to shut down idle adiabatic combinational logic blocks. A power-gating scheme for adiabatic combinational circuits has been also presented using ECRLcombinational circuitwith four-phase power-clocks. However, the adiabatic data-retention reported in used more transistors because of its four-phase scheme. In this paper, we propose adiabatic combinational circuit, which are realized with the PFAL and ECRL circuits using four-phase power-clocks. Since clocking schemes and signal waveforms of the four-phase adiabatic combinational circuit ones, power-gating switches and schemes should be also different. Thus, a power-gating scheme for adiabatic combinational circuit using four-phase power-clocks is also presented. All circuits are verified using TSMC 0. 25µm CMOS technology.

II.ADIABATIC SWITCHING

A.Conventional Charging

The dominant factor in the dissipation of a CMOS circuit is the dynamic power required to charge capacitive signal nodes within the circuit. Fig. 1 shows a basic CMOS inverter, together with an equivalent circuit of the charging mechanism. Fig. 2 shows the voltage waveforms present when the input of the inverter swings from high to low, causing the capacitor C to begin charging. At the instant of switching, the full supply potential appears across the on-resistance R of the p-type devicethe waveform then decays as the capacitor is charged to supply. To charge the signal node capacitance c from a supply of potential V_{dd}, a charge $Q = CV_{dd}$is taken from the supply through the p-type device. The total energy $E_T = QV_{dd} = CV_{dd}^2$. Only half of the energy is applied to storing the signal on the capacitor-the other $\frac{1}{2} CV_{dd}^2$, is dissipated as heat, primarily in the device on-resistance R. Note that the dissipation is independent of this resistance: it is a result of the capacitor charge being obtained from a constant voltage source V_{dd}. To drive the inverter output low, the n-type device is used to discharge the $\frac{1}{2} CV_{dd}^2$energy stored in capacitor C by short circuiting the capacitor and dissipating energy as heat. Hence, the total charge/discharge cycle has required an energyCV_{dd}^2,-half being dissipated in

charging, and half being used for information storage before it too is dissipated during discharge [1-4].

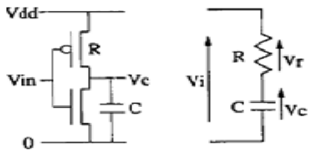

Fig. 1 A Static CMOS inverter and its equivalent circuit for the case where the capacitor C is being charged through a device of on-resistance R.

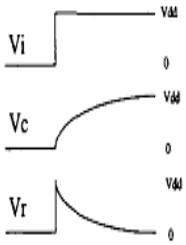

Fig. 2 Voltage waveforms present in the equivalent circuit when charging the capacitor from 0 V to supply in the conventional manner.

B.Adiabatic Charging

Adiabatic switching [5-8] can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. In Fig. 2, it can be seen that the potential V, across the switch Resistance is high in the conventional case because of the abrupt application of V_{dd} to the RC circuit. Adiabatic charging may be achieved by charging the capacitor from a time-varying source, as shown in Fig. 3. This source has an initial value ofV_i = 0 V the ramp increases towardsV_{dd} at a slow rate that ensures $V_r = V_i - V_c$, is kept arbitrarily small. This rate is set by ensuring that the period of the ramp T>>RC.

The energy for a charging event is calculated by Integrating the power p (t) during the transition time T

$$E = \int_0^T p(t)dt = \int_0^T \vartheta(t).\, i(t)dt$$

In fact, the energy dissipated is

$$E_{diss} = I^2\, RT = \left(\frac{CV_{dd}}{T}\right)^2 RT = \left(\frac{RC}{T}\right)CV_{dd}^2$$

A linear increase in T causes a linear decrease in power dissipation. Adiabatic discharge can be arranged in a similar manner with a descending ramp. Now, if T is sufficiently larger than RC, energy dissipation during charging$E_{diss} \rightarrow 0$, and so the total energyremovedfrom the supply is the$\frac{1}{2}CV_{dd}^2$ minimum required to charge the capacitor and hence hold the logic state. This energy may be removed from the capacitor and returned to the power supply adiabatically by rampingV_i, back down from V_{dd} to 0 V. As a result, given a suitable supply, it should be possible then to charge and discharge signal node capacitances with only marginal net losses. Note that the RC time constant of a typical CMOS process is about 20ns.

Fig. 3 Voltage waveforms present in the equivalent circuit when charging the capacitor from 0V to V_{dd} in the adiabatic manner.

III. ADIABATIC LOGIC FAMILIES

In my literature survey practical adiabatic families can be classified as either PARTIALLY ADIABATIC or FULLY ADIABATIC. In a PARTIALLY ADIABATIC CIRCUIT, some charge is allowed to be transferred to the ground, while in a FULLY ADIABATIC CIRCUIT, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic circuitsfacea lot ofproblemswith respect to the operating speedand the inputs power clock synchronization [10-11]. Now I can choose the partial adiabatic circuits i.e., ECRL (Energy Charge Recovery Logic) and PFAL (Positive Feedback Adiabatic Logic).

A.Efficient Charge Recovery Logic(ECRL)

Efficient Charge Recovery Logic (ECRL) proposed by Moon and Jeong, shown in Fig 4, uses cross-coupled PMOS transistors. It has the structure similar to Cascode Voltage Switch Logic (CVSL) with differential signaling. It consists of two cross-coupled transistors and two pull down transistors in the N-functional blocks for the ECRLadiabatic logic block.

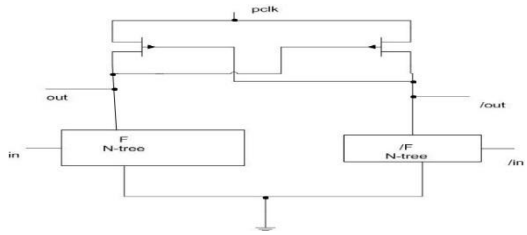

Fig. 4 Basic Structure of Adiabatic ECRL Logic

B.Positive Feedback Adiabatic Logic(PFAL)

The partial energy recovery circuit structure named Positive Feedback Adiabatic Logic (PFAL) has been used, since it shows the lowest energy consumption if compared to other similar families, and a good robustness against technological parameter variations. It is a dual-rail circuit with partial energy recovery. The general schematic of the PFAL gate is shown in Figure 5. The core of all the PFAL[5-6] gates is an adiabatic amplifier, a latch made by the

two PMOS cross coupled transistors and two NMOS transistors,that avoids a logic level degradation on the output nodes out and /out. The two n-trees realize the logic functions.

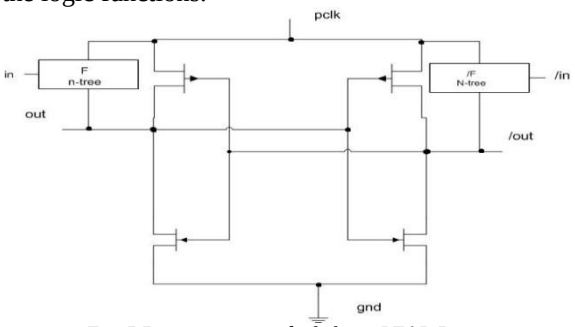

Fig. 5 Basic structure of adiabatic PFAL Logic

IV. DESIGN OF COMBINATIONAL CIRCUIT USING ADIABATIC LOGIC FAMILIES

Based on the basic structures of adiabatic ECRL [9] logic, I can design the ECRL combinational circuit. Initially, input A is high and input B is low. When power clock (pclk) rises from zero to V_{DD} then output carry remains ground level. Output sum follows the pclk. When pclk reaches at V_{DD}, outputs sum and carry hold logic value V_{DD} and zero respectively. This output values can be used for the next stage as an inputs. Now pclk falls from V_{DD} to zero, high outputs returns its energy to pclk hence delivered charge is recovered.

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V. PARAMETER VARIATIONS ONPOWER CONSUMPTION

Power consumption in adiabatic circuits strongly depends on the parameter variations. The impact of parameter variations on the power consumption for the two logic families is investigated with respect of CMOS logic circuit, by means of TSPICE simulations. Simulations are carried out at 250nm technology node.

A. Transition Frequency Variation

Fig.6 shows the power dissipation per cycle versus switching frequency of the two adiabatic logic families and CMOS for the combinational circuit logic. It is seen that for high frequency the behavior is no more adiabatic and therefore the power dissipation increases. Thus the simulations are carried out only at useful range of the frequencies to show better result with respect to CMOS.

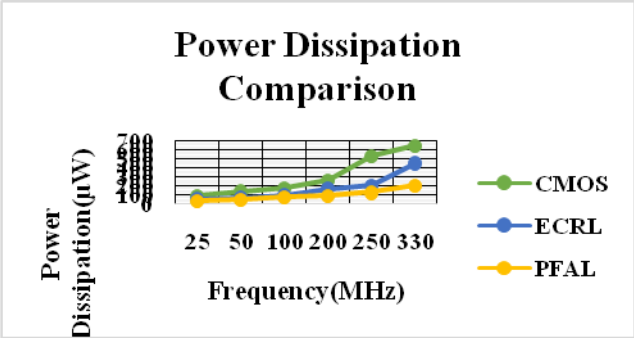

Fig. 6 Power consumption per cycle versus frequency for acombinational circuit
At V_{DD} = 2.5V

B. Supply Voltage Variation

Fig.7 shows the power dissipation per cycle versus supply voltage of the two adiabatic logic families and CMOS for the combinational circuit. It is seen that supply voltage decreases, the gap between CMOS and logic families is reduced. But ECRL and PFAL still shows large power savings over wide range of supply voltage.

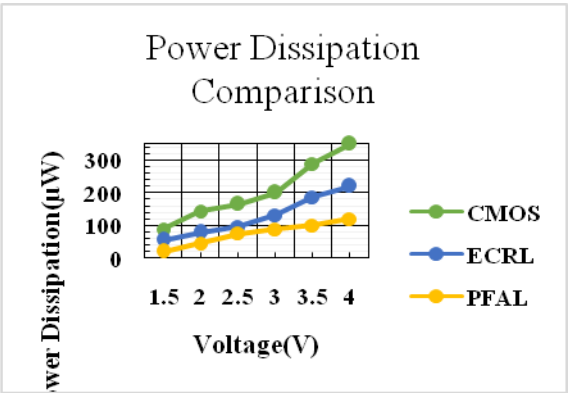

Fig. 7 Power consumption per cycle versus frequency for a combinational circuit At frequency= 100MHz

VI. SIMULATION AND RESULTS

In the below schematic waveform of CMOS combinational circuit is shown in below figure 8.

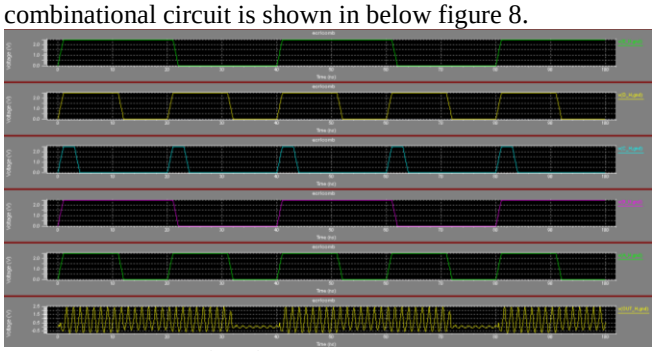

Fig. 8 Simulated waveform for the CMOS Combinational circuit

In the below schematic waveform of ECRLcombinational circuit is shown in below figure 9.

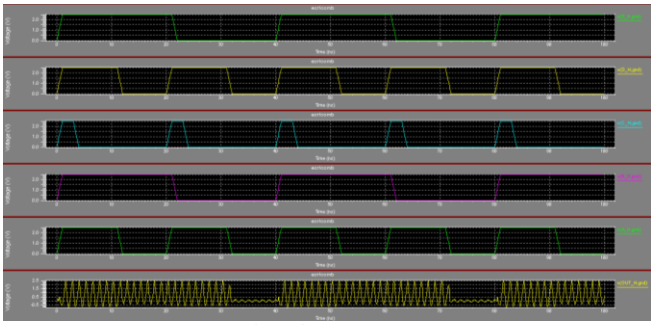

Fig. 9 Simulated waveform for Adiabatic ECRL Combinational circuit.

In the below schematic waveform of PFAL combinational circuit is shown in below figure 10.

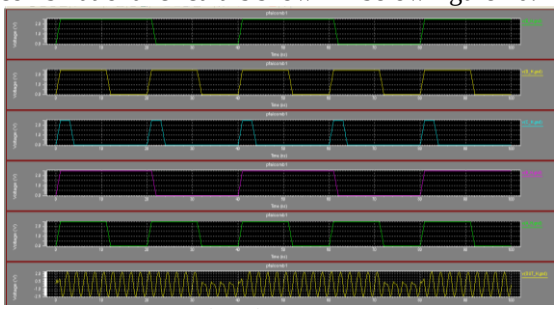

Fig. 10 Simulated waveform for Adiabatic PFAL Combinational circuit.

	NO .OF GATES	POWER DISSIPATION	SUPLLY VOLTAGE
CMOS	6 PMOS, 6 NMOS	26 µW	2.5V
ECRL	2 PMOS, 10 NMOS	5 µW	2.5V
PFAL	2 PMOS, 12 NMOS	1µW	2.5V

TABLE 1 Comparison Power Dissipation at the frequency 100MHz

VII.CONCLUSION

Large scale system development using adiabatic technologies is more complex than conventional CMOS circuit development because of data synchronization and simulation issues Moreover adiabatic circuits have largelatencies due to the dynamic nature of their gates. In this paper adiabatic technique is best for the design the low power circuits from the above results. In this paper design the low power combinational circuit by using ECRL and PFAL. In adiabatic switching principle a power-clock supply plays an important role in adiabatic switching. Hence adiabatic logic families can be used for low power application over the wide range of parameter variation that is frequency and supply voltage.

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